REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated February 27, 2004. Appreciation is expressed to the Examiner for the indication of allowable subject matter in claims 8 and 36.

By the present Amendment, claim 8, indicated as containing allowable subject, has been rewritten as new independent claim 63, including all subject matter of the original claim 8. Therefore, entry and allowance of newly presented claim 63 is respectfully requested.

Also by the present Amendment, claim 32 has been amended to clarify the language regarding the output of the instruction processor to first and second decoders. Therefore, reconsideration and removal of the 35 U.S.C. § 112, second paragraph, rejection of claim 32 is respectfully requested. With regard to claim 9, also rejected under 35 U.S.C. § 112, second paragraph, this claim has been deleted, without prejudice to the Applicants' right to proceed with the subject matter of this claim in a subsequent application. In addition, independent claims 1 and 52 have been cancelled and replaced by new independent claims 64 and 65, as will be discussed below.

Reconsideration and allowance of independent claims 64, 65 and 32, and their respective dependent claims, over the cited primary reference to Black (USP 5,619,408) is respectfully requested. These independent claims particularly define features of the present invention regarding the operation of an instruction processor

and first and second processors when instructions other than specified instructions are received.

For example, in independent claim 64 (replacing claim 1), it is particularly defined that:

> "when specified instructions are received, the information processor outputs the inputted instructions to a second instruction decoder so that the instructions can be performed by a second processor; and
>
> when instructions other than the specified instructions are received, a first instruction, different from the inputted instruction, is output from the instructions processor to a second instruction decoder wherein the instructions other than said specified instructions are decoded by the first instruction decoder and performed on by the first processor."

As such, in accordance with the invention defined in claim 64, when the instructions are not the specified instructions, the information processor will provide a first instruction, different from the inputted instructions, to the second decoder, and, meanwhile, the instructions themselves are decoded by a first instruction decoder and performed on by the first processor.

In the reference to Black, on the other hand, an IDR logic circuit 46 is provided which recodes each of three noneffective instructions to provide a no-op instruction format, as described on column 6, line 40 of the Black reference. With regard to this, it is noted that the recoding process is performed in common to all of the execution units. As a result, the noneffective instructions are not supplied to any of the execution units. This is in direct contrast to claim 61 which defines that, even when instructions other than the specified instructions are received, they are still decoded by the first instruction decoder and performed on by the first processor (rather than not being performed on at all, as is the case in Black). Therefore, it is

respectfully submitted that new independent claim 64 clearly defines over the Black reference, and reconsideration and allowance of this claim is respectfully requested.

With regard to claim 65, this claim also defines first and second instruction decoders and first and second processors operating in conjunction with either an input instruction or a first instruction which is different from the input instructions. Again, the claim defines two different types of instructions, with one of the instructions being performed on by the first processor and the other of the instructions being performed on by the second processor. Again, this is in direct contrast to Black, which, as described above, provides an arrangement in which none of the instructions are performed on by the processors.

With regard to amended claim 32, this claim also defines first and second decoders and first and second processors coupled, respectively, thereto. In claim 32, it is indicated that when the instruction inputted from the cache memory is not an instruction to perform calculations in the first processor, the instruction processor circuit will output the instruction inputted from the cache memory to the first decoder, and the instruction that is different from the inputted instruction will be provided from the cache memory to the second decoder. Again, there is nothing in the Black reference which suggests this.

For the reasons set forth above, reconsideration and allowance of newly presented independent claims 64 and 65, as well as amended claim 32, over the cited reference to Black, together with allowance of the various dependent claims in this application, is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the

Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 501.38642X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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